

REMARKS

This application has been reviewed in light of the Office Action dated October 29, 2008. Claims 1-8, 12 and 13 are presented for examination, of which Claims 1, 12 and 13 are in independent form. Claim 4 has been amended to correct a typographical error. Favorable reconsideration is respectfully requested.

In the Office Action, Claims 1-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,180,870 (Sano et al.) in view of U.S. Patent 5,021,100 (Ishihara et al.) further in view of Japanese Patent 2000-150934 (Nakajima et al.), and Claims 12 and 13, as being unpatentable over *Ishihara* in view of U.S. Patent 6,468,885 (Mahan et al.).

As discussed in the specification and in the Amendment of July 29, 2008, passivation is generally an effective means for treating electrical defects leading to decreased shunt resistance (para. [0010]). However, in a stacking configuration (“stacking configuration of interest” hereafter) with a unit photovoltaic element (UPE) near the substrate, a UPE close to the light incidence point, and an intermediate transmission/reflection (ITR) layer, such as an ZnO layer, between the two UPEs, passivation normally could not reach the UPE near the substrate. This means that even with passivation treatment, defect-induced short-circuit current would continue to spread laterally from the UPE near the substrate to the ITR layer and thus flow through the UPE near the substrate to decrease the electromotive force.

The present invention has been made to address this issue by offering an ITR layer with a higher resistivity on its substrate side – the side in contact with the UPE near the substrate – than on its light-incident side – the side in contact with the UPE close to the light-incident point – to curb the lateral spreading of defect-induced short-circuit current from the UPE near the substrate to the ITR layer (para. [0052], for example). Applicants note the significance

of the way the resistivity of the ITR layer changes with respect to the stacking configuration of interest, as the way the resistivity varies is in direct response to the nature of the stacking configuration of interest.

Claim 1 recites, among other features, “a resistivity of the zinc oxide layer on the surface in contact with a unit photovoltaic element near a substrate as seen from the zinc oxide layer is higher than a resistivity of the zinc oxide layer on the surface in contact with a unit photovoltaic element farther from the substrate as seen from the zinc oxide layer.”

The feature recited above is not believed to be disclosed or suggested in *Sano*, *Ishihara*, and *Nakajima*, considered separately or in any permissible combination. While conceding that the feature “the resistivity of the zinc oxide layer varying in the direction of its thickness” is not disclosed or taught in *Sano* and/or *Ishihara*, the Office Action states that it is in *Nakajima*. The Office Action appears to further suggest that the feature of Claim 1 recited in the last paragraph is obvious from the combination of *Sano*, *Ishihara*, and *Nakajima*. Applicants respectfully disagree.

As discussed previously, *Nakajima* does not concern the stacking configuration of interest. Similar to *Sano*, it instead deals with a configuration having a diffusion-prevention layer (or a transparent conductive layer – possessing good multifunctional control of optical and electrical properties – such as a ZnO layer) between an amorphous silicon thin-film cell in a p-i-n structure (a-Si layer) of one UPE and a reflective metal layer (*see* Fig. 1). Specifically, it aims to provide a good transparent conductor, where the side in contact with the a-Si layer has a higher impurity and thus lower resistivity, making a good junction (for electricity), and the side in contact with the reflective metal layer has a lower impurity and thus higher transmittance, making it easier for light to pass through (*see* Abstract).

Even if *Nakajima* is deemed to disclose the feature “the resistivity of the zinc oxide layer varying in the direction of its thickness” or specifically *lowering the resistivity* on the side of the zinc oxide in contact with an a-Si layer of one UPE *with its other side in contact with a reflective metal layer*, Applicants see no reason why one of ordinary skill in the art at the time of the present invention would have considered applying this feature to *increase the resistivity* on the side of an ITR layer in contact with a UPE near the substrate side *with its other side in contact with a UPE close to the light incidence point*. Certainly, none of *Sano*, *Ishihara*, and *Nakajima* discusses the issue that this invention has been made to address, which arises specifically from the stacking configuration of interest. Starting with the combination of *Sano*, *Ishihara*, and *Nakajima*, it would have been a substantial conceptual leap to implement all of the features recited in Claim 1.

Accordingly, for at least the reasons noted above, Claim 1 is believed to be allowable over *Sano*, *Ishihara*, and *Nakajima*, considered separately or in any combination.

More broadly speaking, the two sides of an ITR layer disclosed in the present invention are functionally separate from each other (para. [0066]), which is manifested in differing resistivity and other aspects as well. There are various considerations that can go into the creation of an optimum ITR layer for the stacking configuration of interest.

As an example, while it is necessary for the light-incident side of the ITR layer to have good characteristics, this requirement does not necessarily hold for the substrate side (para. [0067]). Therefore, it is helpful to apply a technique such as using a higher deposition rate, which while liable to degraded characteristics is economically advantageous, to the substrate side of the ITR layer.

On the other hand, it is possible to use different kinds of material respectively for the two sides of an ITR layer disclosed in the present invention. For example, the light-incident side of the ITR layer could be an In_2O_3 layer, and the substrate side could be a ZnO layer (para. [0058]). There are several reasons why it is preferable to have the In_2O_3 layer formed at a higher temperature than the ZnO layer (para. [0068]). Therefore, it is helpful to use a lower deposition temperature for the substrate side of the ITR layer.

Applicants note that whether it is adjusting the deposition rate or adjusting the deposition temperature, such an adjustment is applicable specifically to the deposition of an ITR layer, normally with ZnO and/or In_2O_3 , in the stacking configuration of interest and is motivated by an independent set of reasons. A bottom line is that the adjustment would contribute to the creation of an optimum ITR layer in the stacking configuration of interest – certainly not that the deposition rate and the deposition temperature would somehow be related to each other and affect the formation of the ITR layer in a joint manner.

Claim 12 recites, among other features, that “the second layer is formed at a rate higher than that of the first layer [where the second layer is the substrate side of the ITR layer].” Similarly, Claim 13 recites, among other features, that “the second layer is formed at a temperature lower than that of the first layer.”

The features recited above are not believed to be disclosed or suggested in *Ishihara* or *Mahan*, considered separately or in any permissible combination. While conceding that these features are not disclosed or suggested in *Ishihara*, the Office Action states that they are in *Mahan*. Applicants respectfully disagree.

The portion of *Mahan* cited in the Office Action as disclosing the features recited above describes merely how the deposition rate and the *substrate temperature* affect the

hydrogen content in the decomposition of the silicohydride gas for fabricating an a-Si:H layer to be used as semiconductor material. It does not at all discuss how the deposition rate and the *deposition temperature* may separately affect the formation of an ZnO or In₂O₃ layer to be used as an ITR layer in the stacking configuration of interest. Certainly, it does not disclose “the second layer is formed at a rate higher than that of the first layer,” as recited in Claim 12 or “the second layer is formed at a temperature lower than that of the first layer,” as recited in Claim 13.

Applicants also do not see any reason why someone with ordinary skill in the art at the time of the present invention would consider applying the *Mahan* technique for fabricating an a-Si:H layer for use as semiconductor material to the formation of an ZnO or In₂O₃ layer to be used as an ITR layer in a stacking configuration of interest. Starting with the combination of *Ishihara* and *Mahan*, it would have been a substantial conceptual leap to implement all of the features recited in Claims 12 and 13.

Accordingly, for at least the reasons noted above, Claims 12 and 13 are believed to be allowable over *Ishihara* and *Mahan*, considered separately or in any combination.

A review of the other art of record has failed to reveal anything which, in Applicants' opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual reconsideration of the patentability of each on its own merits is respectfully requested.

This Amendment After Final Action is believed clearly to place this application in condition for allowance and its entry is therefore believed proper under 37 C.F.R. § 1.116. In any event, however, entry of this Amendment After Final Action, as an earnest effort to advance prosecution and reduce the number of issues, is respectfully requested. Should the Examiner believe that issues remain outstanding, he is respectfully requested to contact Applicant's undersigned attorney in an effort to resolve such issues and advance the case to issue.

In view of the foregoing amendments and remarks, Applicants respectfully request favorable reconsideration and early passage to issue of the present application.

Applicants' undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,

/Leonard P Diana/
Leonard P. Diana
Attorney for Applicants
Registration No.: 29,296

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200